# F8213

## NFC Forum Type 2 Tag compliant IC with 144 bytes user memory

## Functional Specification

V1.02

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Shanghai Feiju Microelectronics Co., Ltd.

ADD: Bulding 13,299 Bisheng Road,Zhangjiang Hi-TechPark,

Pudong District,Shanghai,China (201204)

Tel：86-21-58599366　Fax：86-21-68391075

http://www.nfcic.com

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# 1. Features

## RF interface

Contactless transmission of data and supply (no battery needed)

Operating frequency: 13.56MHz

Fast communication baud rate: 106Kbit/s

Contactless transmission of data and supply (no battery needed)

Operating distance: up to 100mm (depending on antenna geometry)

Half duplex communication protocol using handshake

Typical transaction time: ＜100ms

High data integrity: 16-bit CRC, parity, bit coding, bit counting

True anticollision

7 byte serial number (cascade level 2 according to ISO/IEC 14443-3)

ECC based originality signature

Fast read command

UID ASCII mirror for automatic serialization NDEF messages

Automatic NFC counter triggered at read command

NFC counter ASCII mirror for automatic adding actual read counter value to the NDEF message

## EEPROM

180 bytes organized in 45 pages with 4 bytes per page

144 bytes freely available user Read/Write area (36 pages)

4 bytes initialized capability container with one time programmable access bits

Field programmable read-only locking function per page for the first 16 pages

Field programmable read-only locking function above the first 16 pages per double page for F8213

Configurable password protection with optional limit of unsuccessful attempts

Anti-tearing support for capability container (CC) and lock bits

ECC supported originality check

Data retention time of 10 years

Write endurance 100.000 cycles

## High security

Anti-cloning support by unique 7-byte serial number for each device

32-bit user programmable OTP area

Field programmable read-only locking function per page for first 512 bits

Read-only locking per block for rest of memory

### High Reliability

Endurance: 100,000cycle

Data Retention: 10 Years

### Cascaded UID

The anticollision function is based on an IC individual serial number called Unique IDentifier. The UID of the F8213 is 7 bytes long and supports cascade level 2 according to ISO/IEC 14443-3.

### Anticollision

An intelligent anticollision function according to ISO/IEC 14443 allows to operatemorethan one card in the field simultaneously. The anticollision algorithm selects each cardindividually and ensures that the execution of a transaction with a selected card isperformed correctly without data corruption resulting from other cards in the field.

# 2. Product Overview

## 2.1 Introduction

F8213 is NFC Forum Type 2 Tag compliant IC according to ISO14443 Type A development by Shanghai Feiju Microelectronics Co., Ltd.TheF8213 chip consists of the 168 bytes of the total memory organized in 42 usermemory EEPROM. From that amount, 144 bytes (36 pages) are available for the userdefined data.

Along with the memory,F8213 contains the RF-Interface and the Digital Control Unit. Energy and data are transferred via an antenna, which consists of a coil with a few turns directly connected to the RF1 and RF2 of the F8213. No furtherexternal components are necessary.

## 2.2 Block Diagram

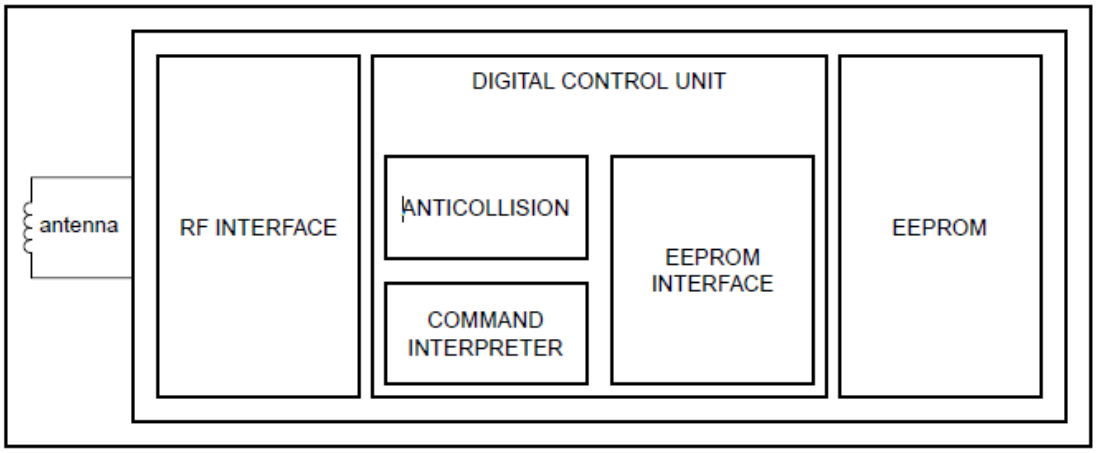



Figure 1 F8213 Block Diagram

# 3. Functional description

## 3.1 Block description

RF Interface:

- modulator/demodulator
- rectifier
- clock regenerator
- POR
- voltage regulator

Anticollision: multiple cards may be selected and managed in sequence

Command interpreter: processes memory access commands

EEPROM interface: 180bytes, organized in 45 pages

## 3.2 State diagram and logical states description

Commands are initiated by the NFC device and controlled by the F8213 command interpreter. This processes the internal states and generates the appropriate response.

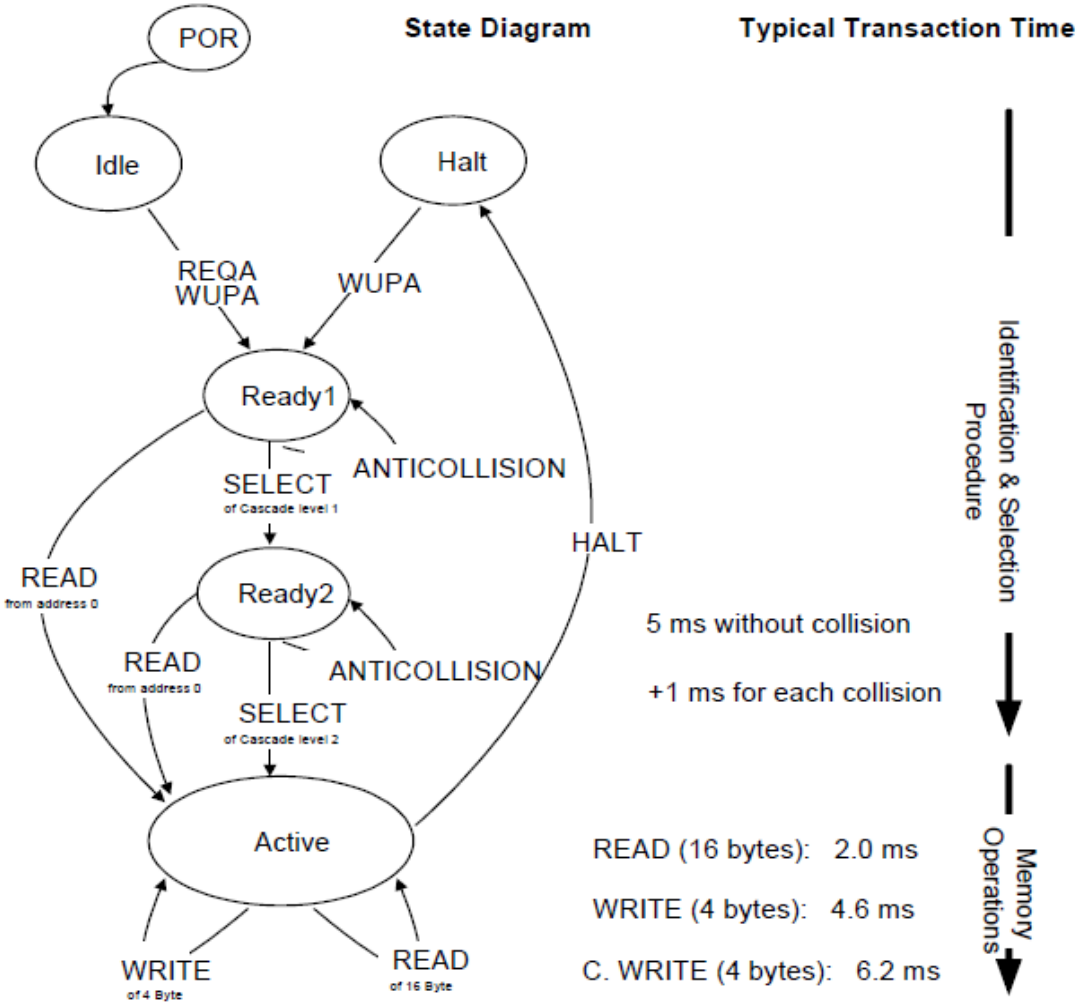



Fig 2. Communication principle state diagram - 4-byte; 16-byte

## 3.2.1Idle state

After a Power-On Reset (POR), the F8213 switches directly to the idle state. It only exits this state when a REQA or a WUPA command is received from the NFC device. Any other data received while in the idle state is interpreted as an error and the F8213 remains Idle.

## 3.2.2Ready1 state

In this state, the F8213 supports the NFC device when resolving the first part of its UID (3 bytes) with the ANTICOLLISION or SELECT command from cascade level 1. This state is exited correctly after execution of either of the following commands:

• SELECT command from cascade level 1: the NFC device switches F8213 into

Ready2 state where the second part of the UID is resolved.

• READ command (from address 0): all anticollision mechanisms are bypassed and F8213 switches directly to the active state.

**Remark:** If more than one F8213 is in the NFC device field, a READ command from address 0 causes a collision due to the different serial numbers and all F8213 devices are selected. Any other data received in the Ready1 state is interpreted as an error and depending on its previous state the F8213 returns to the wait, idle or halt state.

### 3.2.3 Ready2 state

In this state, the F8213 supports the NFC device when resolving the second part of its UID (4 bytes) with the cascade level 2 ANTICOLLISION command. This state is usually exited using the cascade level 2 SELECT command.

Alternatively, state Ready2 may be skipped using a READ command (from address 0) as described in state Ready1.

**Remark:** If more than one F8213 is in the NFC device field, a READ command from address 0 causes a collision due to the different serial numbers and all F8213 devices are selected. The response of the F8213 to the cascade level 2 SELECT command is the Select Acknowledge (SAK) byte. In accordance with ISO/IEC 14443 this byte indicates if the anticollision cascade procedure has finished. It also defines the type of device selected for the MIFARE architecture platform. The F8213 is now uniquely selected and only this device will communicate with the NFC device even when other contactless devices are present in the NFC device field. Any other data received when the device is in this state is interpreted as an error and depending on its previous state the F8213 returns to the wait, idle or halt state.

### 3.2.4 Active state

In the active state either a 16-byte READ or 4-byte WRITE command can be performed. The HALT command exits either the READ or WRITE commands in their active state. Any other data received when the device is in this state is interpreted as an error and depending on its previous state the F8213 returns to the wait, idle or halt state.

### 3.2.5Halt state

The halt and idle states constitute the second wait state implemented in the F8213. An

already processed F8213 can be set into the halt state using the HALT command. In theanticollision phase, this state helps the NFC device to distinguish between processed cards and cards yet to be selected. The F8213 can only exit this state on execution of the WUPA command. Any other data received when the device is in this state is interpreted as an error and the F8213 state is unchanged. Refer to the document MIFARE collection of currently available application notes for correct implementation of an anticollision procedure based on the idle and halt states and the REQA and WUPA commands.

## 3.3 Data integrity

The following mechanisms are implemented in the contactless communication link between NFC device and F8213 to ensure a reliable data transmission:

• 16 bits CRC per block
• Parity bit for each byte
• Bit count checking
• Bit coding to distinguish between "1", "0", and no information
• Channel monitoring (protocol sequence and bit stream analysis)

## 3.4 RF interface

The RF-interface is according to the standard for contactless smart cards ISO/IEC 14443A .

The RF-field from the NFC device is always present (with short modulation pulses when transmitting), because it is used for the power supply of the card.

For both directions of data communication there is one start bit at the beginning of each frame. Each byte is transmitted with a parity bit (odd parity) at the end. The LSBit of the byte with the lowest address of the selected block is transmitted first. The maximum frame length is 164 bits (16 data bytes + 2 CRC bytes = 16 * 9 + 2 * 9 + 1 start bit + 1 end bit).

## 3.5 Memory organization

The 168 Bytes of the total memory organized in 42 user memory EEPROM. From that amount, 144 Bytes (36 pages) are available for the user defined data. Each page contains 4 Bytes (32 bits). In the erased state the EEPROM cells are read as a logical “0”, in the

written state as a logical “1”.

| Page address | | Byte number | | | |
|---|---|---|---|---|---|
| Decimal | Hex | 0 | 1 | 2 | 3 |
| 0 | 00h | serial number | | | |
| 1 | 01h | serial number | | | |
| 2 | 02h | serial number | internal | lock bytes | lock bytes |
| 3 | 03h | OTP | OTP | OTP | OTP |
| 4 to 39 | 04h to 27h | user memory | user memory | user memory | user memory |
| 40 | 28h | lock bytes | lock bytes | - | - |
| 41 | 29h | 16-bit counter | 16-bit counter | - | - |

Table 2 F8213Memory organization

## 3.5.1 UID/serial number

The unique 7 byte serial number (UID) and its two Block Check Character Bytes (BCC) are programmed into the first 9 bytes of the memory. It therefore covers page 00h, page 01h and the first byte of page 02h. The second byte of page 02h is reserved for internal data. Due to security and system requirements these bytes are write-protected after having been programmed by the IC manufacturer after production.

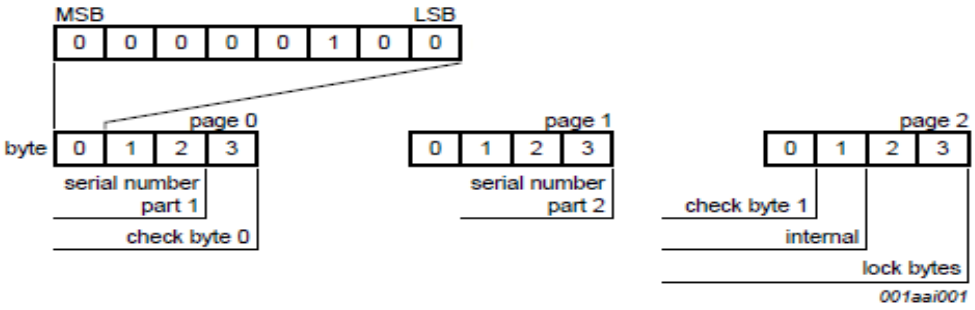



Fig3 UID/serial number

According to ISO/IEC 14443-3 BCC0 is defined as CT⊕SN0⊕SN1⊕SN2.Abbreviations CT stays for Cascade Tag byte (88h) and BCC1 is defined as SN3⊕SN4⊕SN5⊕SN6. SN0 holds the Manufacturer ID for FEIJU (53h) according to ISO/IEC 14443-3 and ISO/IEC 7816-6 AMD.1.

## 3.5.2 Lock bytes

Lock bytes enable the user to lock parts of the complete memory area for writing. A Read from user memory area cannot be restricted via lock bytes functionality.

The lock bytes functionality is enabled with a WRITE command (see Section 8.8.7

"WRITE") or COMPATIBILITY WRITE command (see Section 8.8.8 "COMPATIBILITY WRITE"), where 2 out of 4 bytes transmitted are used for setting the lock bytes. Two corresponding bytes - either bytes 2 and 3 for page 02h or bytes 0 and 1 for page 28h - and the actual content of the lock bytes are bit-wise "OR-ed". The result of OR operation becomes the new content of the lock bytes. Two unused bytes do not have to be considered. Although included in the COMPATIBILITY WRITE or WRITE command, they are ignored when programming the memory.

| Name | Page | | Function |
|---|---|---|---|
| | Number | Address | |
| Lock byte 0 | 2 | 02h | page and block locking |
| Lock byte 1 | 2 | 02h | page locking |
| Lock byte 2 | 40 | 28h | page and block locking |
| Lock byte 3 | 40 | 28h | functionality and block locking |

Table3 Lock bytes

Due to the built-in bitwise OR operation, this process is irreversible. If a bit is set to "1", it cannot be changed back to "0" again. Therefore, before locking the lock bytes, the user must ensure that the corresponding user memory area and/or configuration bytes are correctly written.

The configuration written in the lock bytes is active upon the next REQA or WUPA command.

The single bits of the 4 bytes available for locking incorporate 3 different functions:

• the read-only locking of the single pages or blocks of the user memory area

• the read-only locking of the single bytes of the configuration memory area

• the locking of the lock bits themselves

For the compatibility reasons, the first 64 bytes (512 bits) of the memory area have the twolock bytes used for the configuration of this memory area are identically configured. Themapping of single bits to memory area for the first 64 bytes (512 bits) is shown in Figure 3-2.The bits of byte 2 and 3 of page 02h represent the field-programmable read-only lockingmechanism. Each page x from 03h (OTP bits) to 0Fh may be locked individually toprevent further write access by setting the corresponding locking bit Lx to 1. After lockingthe page is read-only memory.

The 3 least significant bits of lock byte 0 of page 2 are the block-locking bits. Bit 2 handles pages 0Fh to 0Ah, bit 1 pages 09h to 04h and bit 0 page 03h (OTP bits). Once the block locking bits are set, the locking configuration for the corresponding memory area is frozen.

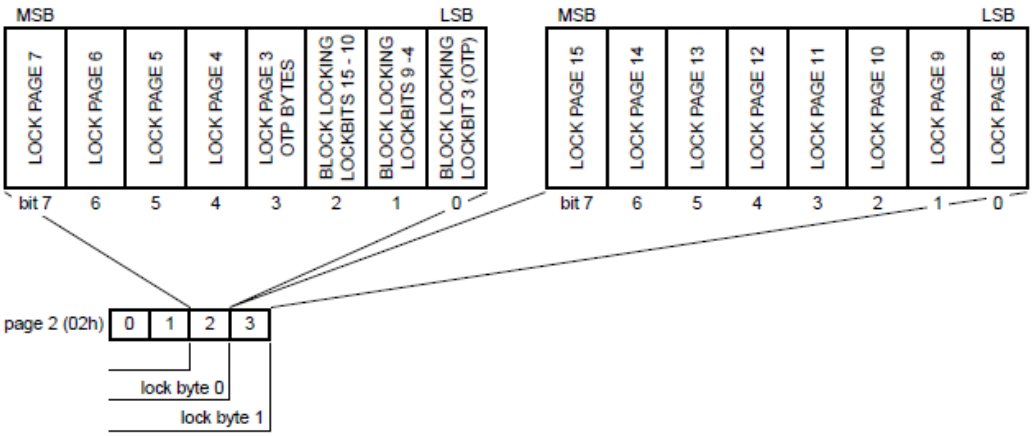



Fig4 Lock bytes 1 and 2

For locking of pages starting at page address 10h onwards, lock bytes located in page 28h are used. Those two lock bytes cover the memory area of 96 data bytes together with configuration area from page address 28h onwards. Therefore, the granularity is larger then for the first 64 bytes as shown in Figure 3-3 “Lock bytes 3 and 4”.

The functionality beyond page address 28h which can be locked read-only is:

• the counter

• the lock bytes themselves

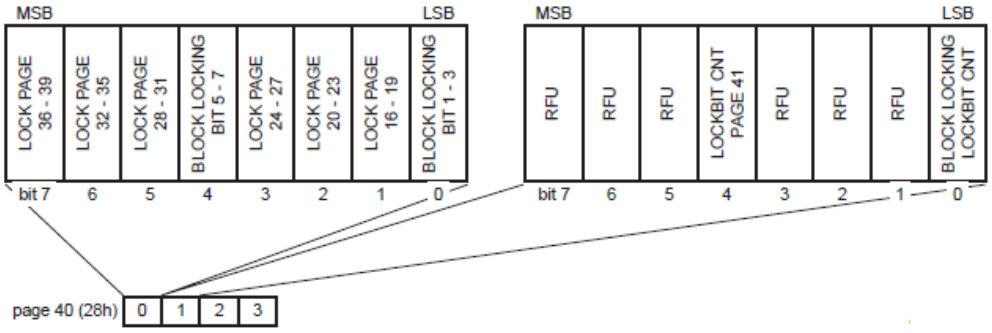
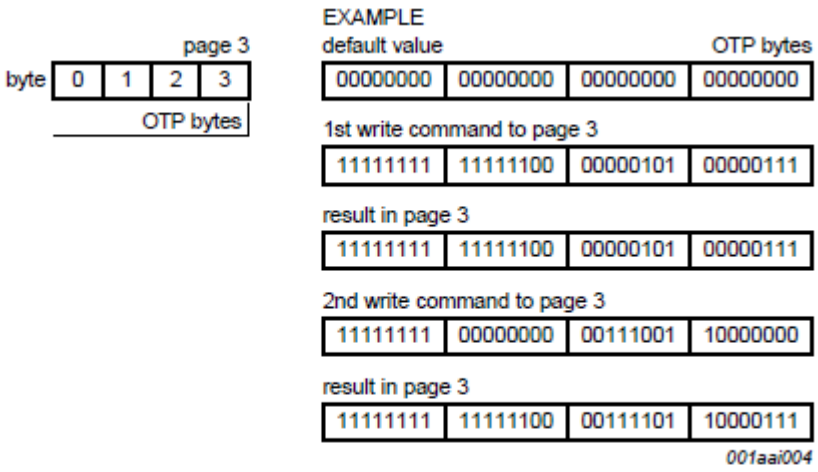



Fig5 Lock bytes 1 and 2

## 3.5.3 OTP bytes

Page 3 is the OTP page. It is preset to all “0” after production. These bytes may be bit-wise modified by a WRITE command.




(1) **Remark:** This memory area may be used as a 32 ticks one-time counter.

Fig6 OTP bytes

The bytes of the WRITE command and the current contents of the OTP bytes are bit-wise "OR-ed" and the result becomes the new content of the OTP bytes. This process is irreversible. If a bit is set to "1", it cannot be changed back to "0" again.

## 3.5.4 Data pages

F8213 features 144 bytes of data memory. The address range from page 04h to 27h constitutes the read/write area.

Initial state of each byte in the user area is 00h.

A write access to data memory is achieved with WRITEorCOMPATIBILITY WRITE command. Inboth cases, 4 bytes of memory (one page) will be overwritten. Write access to datamemory can be permanently restricted via lock bytes.

**NFC Forum Type 2 Tag compliance**

F8213 has been designed to be compliant with NFC Forum Type 2 Tag specification. With its 144 bytes of data memory, it can

easily support use cases like Smart Poster, Handover, SMS, URL or Call Request.

## 3.5.5Initial memory configuration

The memory configuration of F8213 in delivery state is shown in Table 3-3 "Initial memory organization":

| Page address | | Byte number | | | |
|---|---|---|---|---|---|
| dec. | hex. | 0 | 1 | 2 | 3 |
| 0 | 00h | UID0 | UID1 | UID2 | BCC0 |
| 1 | 01h | UID3 | UID4 | UID5 | UID6 |
| 2 | 02h | BCC1 | internal | 00h | 00h |
| 3 | 03h | E1h | 10h | 12h | 00h |
| 4 | 04h | 01h | 03h | A0h | 10h |
| 5 | 05h | 44h | 03h | 00h | FEh |
| 6 to 39 | 06h to 27h | 00h | 00h | 00h | 00h |
| 40 | 28h | 00h | 00h | rfu | rfu |
| 41 | 29h | 00h | 00h | rfu | rfu |

Table4 Initial memory organization

The memory configuration in pages 3 to 5 ensures that F8213 is a NFC forum Type 2 Tag in INITIALIZED state according to the NFC Forum Technical Specification. It is recommended that any furthermodification of the memory pages 2 to 40 should be according to theTag 2 TypeOperation, Technical Specification.

All lock bytes are set to zero meaning that no page or functionality is locked. Counter is set to zero.

## 3.6Counter

F8213 features 16-bit one-way counter, located at first two bytes of page 29h. In its delivery state, counter value is set to 0000h.

The firstvalid Write or Compatibility write to the address 29h can be performed with any value in the range between 0001h and FFFFh and corresponds to initial counter value. Every consequent valid WRITE command, which represents the increment, can contain values between 0001h and 000Fh. Upon such WRITE command and following mandatory RF reset, the value written to the address 29h is added to the counter content.

If after initial write a value higher then 000Fh is used as a parameter, F8213 will answer with NAK. Once counter value reaches FFFFh and an increment is performed via valid command, F8213 will answer with NAK. If the sum of counter value and increment is higher than FFFFh, F8213 will answer with NAK and will not update the counter.

Increment by zero (00h) is always possible, but does not have any impact to counter value.

## 3.7PICC response to a command from NFC device

NFC Tag Type 2 compliant IC uses, apart from the responses defined in the following sections, two half-byte answers to acknowledge the command received in Active state. NFC Tag Type 2 compliant IC distinguishes between positive (ACK) and negative (NAK) acknowledge. Valid values for ACK and NAK are shown in Table 5 “ACK and NAK values”.

| Answer value | Answer explanation |
|---|---|
| Ah | positive acknowledge (ACK) |
| 1h | parity or CRC error (NAK) |
| 0h | any other error (NAK) |

Table 5 ACK and NAK values

After every NAK, F8213 will perform an internal reset.

## 3.8Command set

The ATQA and SAK are identical as information on ISO 14443 cardactivation. Summary of data relevant fordevice identification is given in Section 8.9 “Summary of relevant data fordeviceidentification”.

The F8213 comprises the command set as described in following chapters.

### 3.8.1 REQA

| Code | Parameter | Data | Integrity mechanism | Response |
|---|---|---|---|---|
| 26h (7-bit) | - | - | Parity | 0044h |

Table6 REQA

**Description:** The F8213 accepts the REQA command in Idle state only. The response is the 2-byte ATQA (0044h). REQA and ATQA are implemented fully according to ISO/IEC 14443-3.

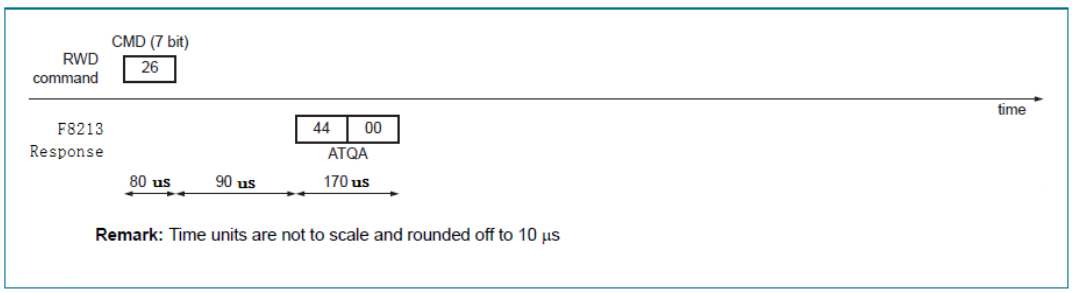



Fig7 REQA

## 3.8.2WUPA

| Code | Parameter | Data | Integrity mechanism | Response |
|---|---|---|---|---|
| 52h (7-bit) | - | - | Parity | 0044h |

Table7 WUPA

**Description:** F8213 accepts the WUPA command in the Idle and Halt state only. The response is the 2-byte ATQA (0044h). WUPA is implemented fully according to ISO/IEC 14443-3.

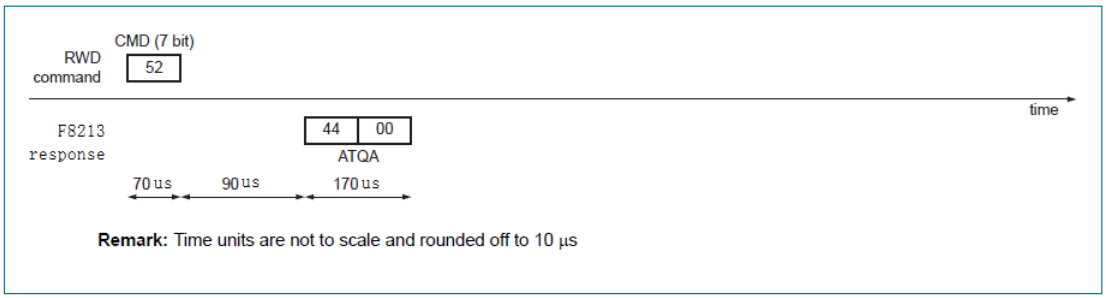



Fig8 WUPA

## 3.8.3ANTICOLLISION and SELECT of cascade level 1

| Code | Parameter | Data | Integrity mechanism | Response |
|---|---|---|---|---|
| Anticollision: 93h | 20h | - | Parity, BCC | - |
| Anticollision: 93h | 21h to 67h | Part of the UID | Parity, BCC | Parts of UID |
| Select: 93h | 70h | First 3 bytes of UID | Parity, BCC, CRC | SAK ('04') |

Table8 ANTICOLLISION and SELECT of cascade level 1

**Description:** The ANTICOLLISION and SELECT commands are based on the same command code. They differ only in the Parameter byte. This byte is per definition 70h in case of SELECT. F8213 accepts these commands in the Ready1 state only. The response is part 1 of the UID. Even with incorrect CRC value, the SELECT command will be fully functional.

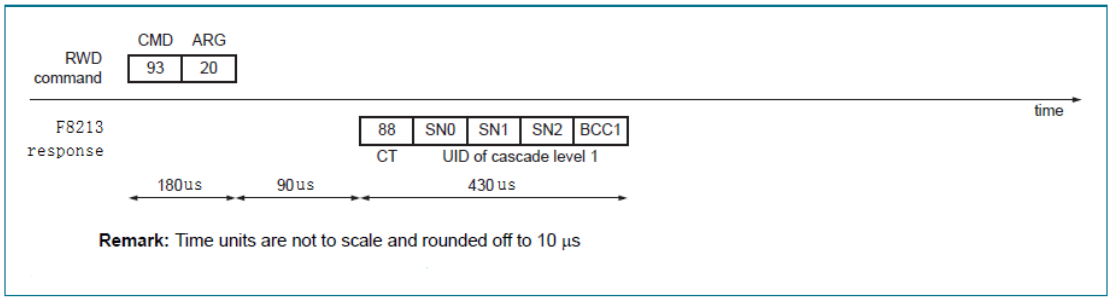



Fig9 ANTICOLLISION and SELECT of cascade level 1

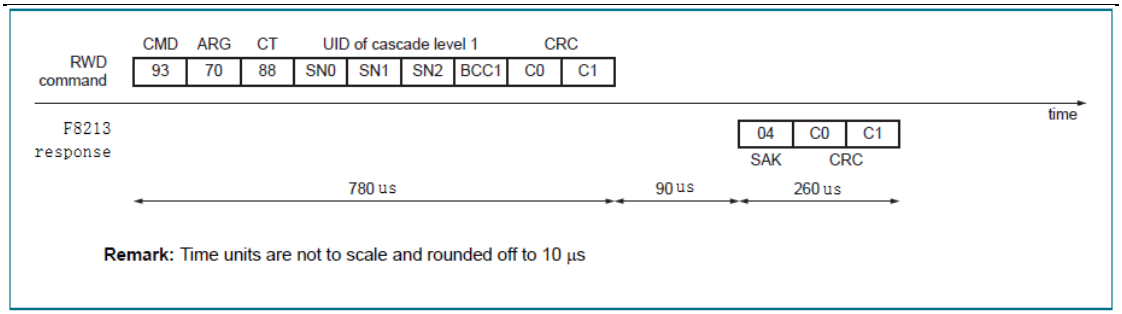



Fig10 SELECT of cascade level 1

## 3.8.4ANTICOLLISION and SELECT of cascade level 2

| Code | Parameter | Data | Integrity mechanism | Response |
|---|---|---|---|---|
| Anticollision: 95h | 20h | - | Parity, BCC | - |
| Anticollision: 95h | 21h to 67h | Part of the UID | Parity, BCC | Parts of UID |
| Select: 95h | 70h | Second 4 bytes of UID | Parity, BCC, CRC | SAK ('00') |

Table9 ANTICOLLISION and SELECT of cascade level 2

**Description:** The ANTICOLLISION and SELECT commands are based on the same command code. They differ only in the parameter byte. This byte is per definition 70h in case of SELECT. F8213 accepts these commands in the Ready2 state only. The response is part 2 of the UID. Even with incorrect CRC value, the SELECT command will be fully functional.

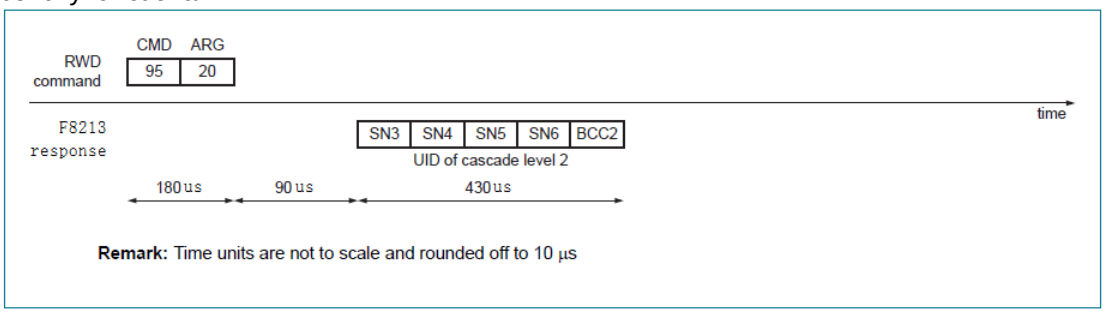



Fig11ANTICOLLISION and SELECT of cascade level 2

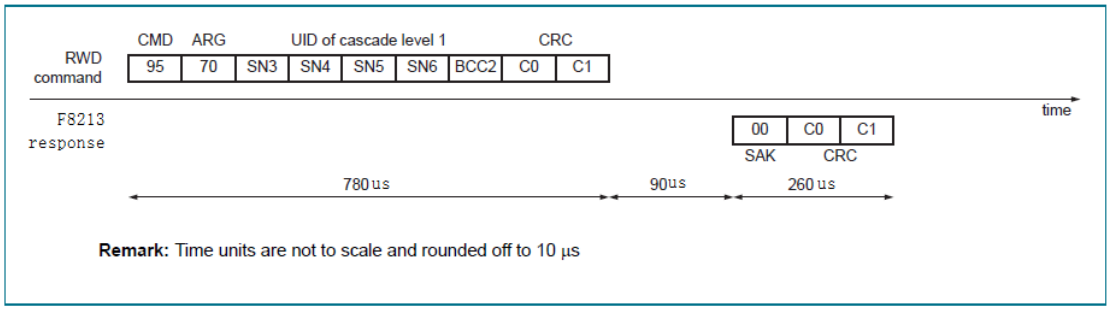



Fig12 SELECT of cascade level 2

## 3.8.5READ

| Code | Parameter/ARG | Data | Integrity mechanism | Response |
|---|---|---|---|---|
| 30h | ADR: '00h' to '29h' | - | Parity, CRC | 16 Byte Date |

Table10 READ

**Description:** The READ command needs the page address as a parameter. Only addresses 00h to 29h are decoded. For higher addresses, F8213 returns a NAK. The F8213 responds to the READ command by sending 16 bytes starting from the page address defined in the command (e.g. if ADR is '03h' pages 03h, 04h, 05h, 06h are returned. If ADR is '29h', the contents of pages 29h, 00h, 01h and 02h is returned).

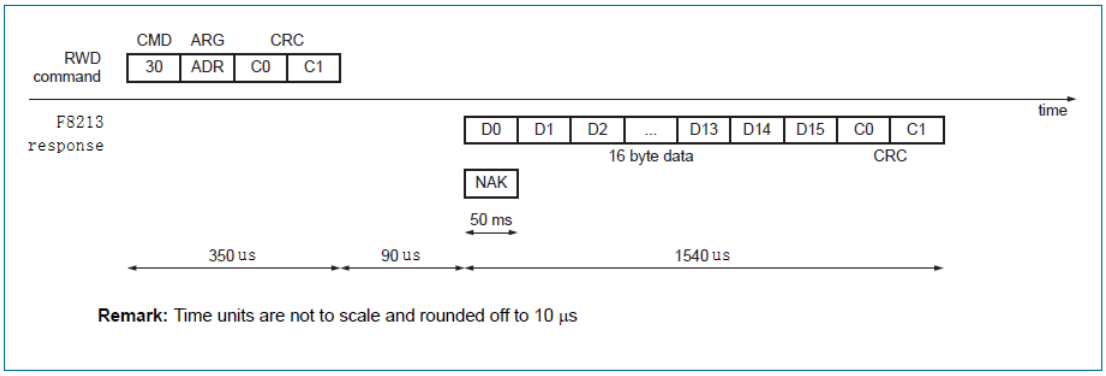



Fig13 READ

## 3.8.6 HALT

| Code | Parameter | Data | Integrity mechanism | Response |
|---|---|---|---|---|
| 50h | 00h | - | Parity, CRC | Passive ACK, NAK |

Table 11 HALT

**Description:** The HALT command is used to set already processed F8213 devices into a different waiting state (Halt instead of Idle), which allows a simple separation between devices whose UIDs are already known (as they have already passed the anticollision procedure) and devices that have not yet been identified by their UIDs. This mechanism is a very efficient way of finding all contactless devices in the field of a NFC device. Even with incorrect parity value, the HALT command will be fully functional.

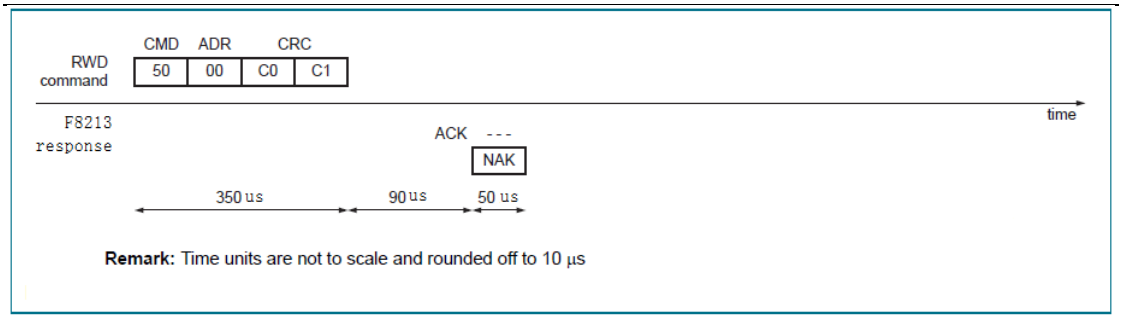



Fig14 HALT

## 3.8.7 WRITE

| Code | Parameter/ARG | Data | Integrity mechanism | Response |
|---|---|---|---|---|
| A2h | ADR: '02h' to '29h' | 4 Byte | Parity, CRC | ACK or NAK |

Table 12 WRITE

Description: The WRITE command is used to program the lock bytes in page 02h, the OTP bytes in page 03h or the data bytes in pages 04h to 05h. A WRITE command is performed page-wise, programming 4 bytes in a page.

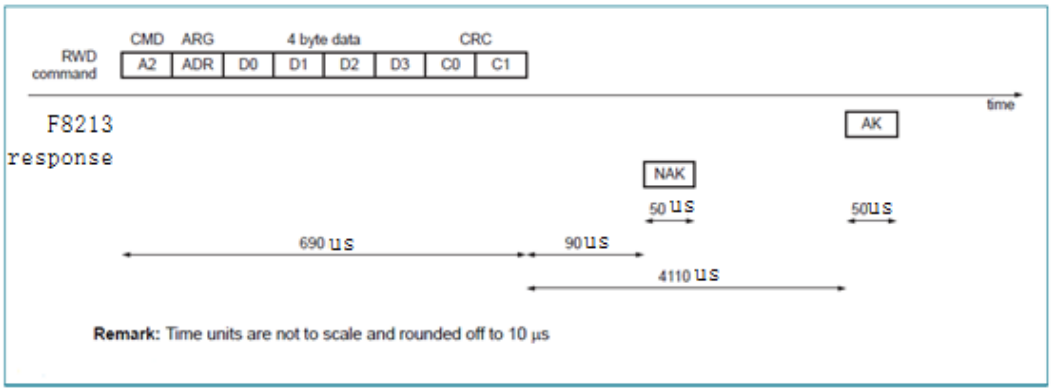



Fig15 WRITE

## 3.8.8COMPATIBILITY WRITE

| Code | Parameter/ARG | Data | Integrity mechanism | Response |
|---|---|---|---|---|
| A0h | ADR: '02h' to '29h' | 16 Byte | Parity, CRC | ACK or NAK |

Fig16 COMPATIBILITY WRITE

**Description:** The COMPATIBILITY WRITE command was implemented to accommodate the established NFC device infrastructure. Even though 16 bytes are transferred to the F8213, only the least significant 4 bytes (bytes 0 to 3) will be written to the specified

address. It is recommended to set the remaining bytes 4 to 15 to all ‘0’.

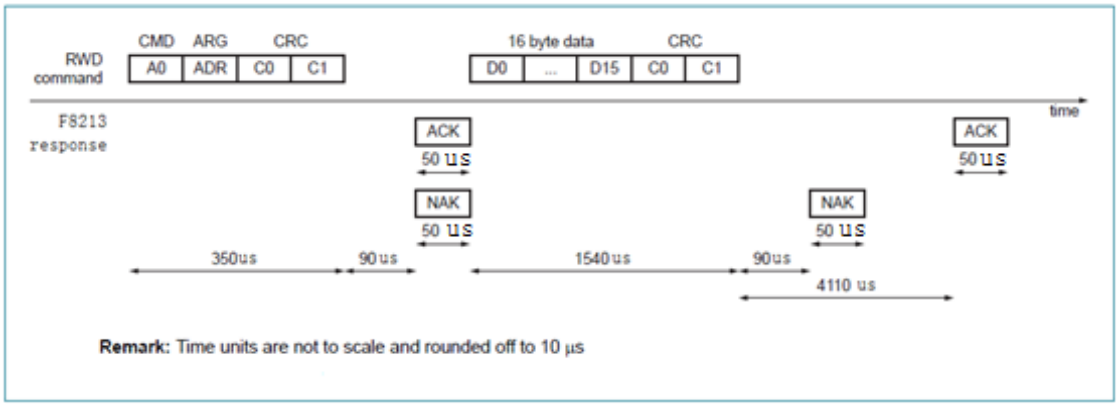



Fig17 COMPATIBILITY WRITE

# 4.ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Cres | Input Capacitance between RF1-RF2 | 47 | 50 | 53 | pF |
| tret | EEPROM Data Retention | 10 | | | Years |
| nwrite | EEPROM Write Endurance | 100000 | | | Cycles |

# 5.OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Tjop | Operatin Junction Temperature | -25 | | 85 | ℃ |
| IRF1-RF2 | Input current | | | 30 | mAms |

# 6.ESD

| SYMBOL | | TEST CONDITIONS | RATING | UNIT |
|---|---|---|---|---|
| Tstg | Storage Temperature Range | | -55 to 130 | ℃ |
| Vesd | ESD Voltrage Immunity | MIL-STD-883C<br>Human Body Model | ±2 | Kv |

MIL Standard 883-C method 3015; Human body model: C = 100 pF, R = 1.5 k.